In the Claims:

1. (Original) An integrated circuit comprising:

conductive patterns formed on a semiconductor substrate;

dielectric patterns disposed between the conductive patterns on the substrate, each having a cross-section with an upside-down T shape and having greater thickness than the conductive patterns;

a nitride film liner lining trenches defined by the conductive patterns and the dielectric patterns;

a dielectric layer on the nitride film liner, filling the trenches; and

at least one metal contact plug passing through the dielectric layer and the nitride film liner and in contact with at least one of the conductive patterns.

2. (Original) The integrated circuit of Claim 1, further comprising:

first and second gates and first and second sources/drains;

a lower dielectric layer formed on the first and second gates and the first and second sources/drains; and

first and second contact plugs each in contact with the first gate and the second source/drain, respectively,

wherein the conductive patterns contact the upper surfaces of the first and second contact plugs.

3. (Original) The integrated circuit of Claim 1, wherein the conductive patterns are bit-line stud pads.

4. (Original) The integrated circuit of Claim 1, wherein the conductive patterns are disposed in a peripheral circuit domain of the semiconductor substrate.

5. (Original) The integrated circuit of Claim 1, wherein the thickness of the nitride film liner is from 100 Å to 1000 Å.

6. (Original) The integrated circuit of Claim 1, further comprising a metal interconnection in contact with the upper surface of the metal contact plug.

7. (Original) An integrated circuit comprising:

conductive patterns formed on a semiconductor substrate in first and second domains;

dielectric patterns disposed between the conductive patterns on the semiconductor substrate, each having a cross-section with an upside-down T shape and having a greater thickness than the conductive patterns;

a nitride film liner lining trenches defined by the conductive patterns and the dielectric patterns;

a dielectric layer in the second domain and filling the trenches;

nitride film studs having insubstantial step difference with respect to the dielectric patterns on the first domain, the nitride film studs covering the upper surfaces of the conductive patterns;

at least one capacitor in contact with a conductive region of the semiconductor substrate and passing through the dielectric patterns;

an intermetal dielectric layer on the capacitor and the dielectric layer; and

at least one metal contact plug in contact with at least one of the conductive patterns and passing through the intermetal dielectric layer, the dielectric layer and the nitride film liner.

8. (Original) The integrated circuit of Claim 7, wherein the first domain is a cell domain and the second domain is a peripheral circuit domain.

9. (Original) The integrated circuit of Claim 7, further comprising:

first and second gates and first and second sources/drains each formed in the second domain;

a plurality of third gates and a plurality of third sources/drains in the first domain;

a lower dielectric layer formed on the first, second and third gates and the first, second and third sources/drains;

first and second conductive pads formed within the lower dielectric layer and contacting a plurality of third source/drains; and

first, second and third contact plugs passing through the lower dielectric layer and in contact with upper surfaces of the first gate,

wherein the conductive pads contact the upper surfaces of the first, second and third contact plugs, and the conductive region includes the upper surface of the first conductive pad.

10. (Original) The integrated circuit of Claim 7, wherein the conductive patterns are bit line stud pads.

11. (Original) The integrated circuit of Claim 7, wherein the thickness of the nitride film liner is from 100 Å to 1000 Å.

12. (Original) The integrated circuit of Claim 7, further comprising a second dielectric layer formed on the nitride film studs, the dielectric patterns and the first dielectric layer, wherein at least one capacitor is formed to pass through the second dielectric layer, and wherein at least one metal contact plug passes through the second dielectric layer.

13. (Original) The integrated circuit of Claim 7, further comprising a metal interconnection in contact with the upper surface of the metal contact plug.

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